PRODUCTION SOLUTION FOR MULTI-GIGABIT DEVICE INTERFACE TEST

ABSTRACT

A ~~special~~ testing method and circuit ~~design is~~ used to test high-speed communication devices on Automatic Test Equipment - ATE. The method and circuit provide ~~It provides~~ a solution to ~~issues in~~ testing very high speed (2.5 Gbps and above) integrated circuits. The circuit fans out the data streams from the output of the Device Under Test (DUT) to multiple tester channels which under-sample the streams. The testing method and circuit ~~design~~ also allow for the injection of jitter into to the DUT ~~part~~ at the output of the DUT ~~device~~. The skipping of data bits inherent in multi-pass testing is avoided by duplicating the tester resources to achieve effective real-time capture (saving test time and improving Bit Error Rate). Moreover the circuit ~~system~~ synchronizes different ~~datacom~~ DUTs with the timing of ATE hardware independent of DUT output data. Also, a calibration method is used compensate for differing trace lengths and propagation delay characteristics of test circuit components.